TSM2301

SOT-23

Pin Definition:
1. Gate
2. Source
3. Drain

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$(mΩ)	I_D (A)
-20	130 @ V_{GS} = -4.5V	-2.8
	190 @ V_{GS} = -2.5V	-2.0

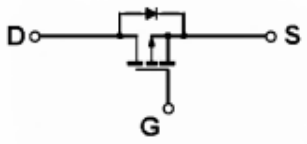
Features

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

Application

- Load Switch
- PA Switch

Block Diagram



P-Channel MOSFET

Ordering Information

Part No.	Package	Packing
TSM2301CX RF	SOT-23	3Kpcs / 7" Reel

Absolute Maximum Rating (Ta = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±8	V
Continuous Drain Current, V_{GS} @4.5V.		I_D	-2.8	A
Pulsed Drain Current, V_{GS} @4.5V		I_{DM}	-8	A
Continuous Source Current (Diode Conduction)[a,b]		I_S	-0.72	A
Maximum Power Dissipation	Ta = 25°C	P_D	0.9	W
	Ta = 75°C		0.57	
Operating Junction Temperature		T_J	+150	°C
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	°C

Thermal Performance

Parameter	Symbol	Limit	Unit
Lead Temperature (1/8" from case)	T_L	5	S
Junction to Ambient Thermal Resistance (PCB mounted)	$R\Theta_{JA}$	120	°C/W

Notes:

a. Pulse width limited by the Maximum junction temperature

b. Surface Mounted on FR4 Board, t ≤ 5 sec.

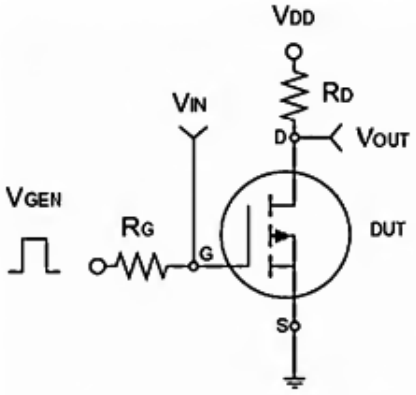
c. Surface Mounted on FR4 Board,

TSM2301

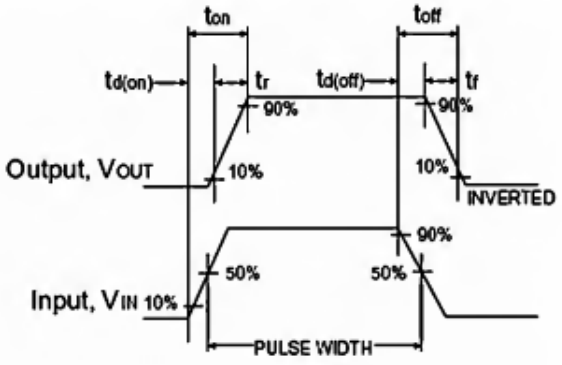
Electrical Specifications (Ta = 25°C unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = -250uA	BV_{DSS}	-20	--	--	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250μA	$V_{GS(TH)}$	-0.45	--	-0.95	V
Gate Body Leakage	V_{GS} = ±8V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V_{DS} = -9.6V, V_{GS} = 0V	I_{DSS}	--	--	-1.0	μA
On-State Drain Current[a]	V_{DS} = -10V, V_{GS} = -5V	$I_{D(ON)}$	-6	--	--	A
Drain-Source On-State Resistance[a]	V_{GS} = -4.5V, I_D = -2.8A	$R_{DS(ON)}$	--	85	130	mΩ
	V_{GS} = -2.5V, I_D = -2.0A		--	122	190	
Forward Transconductance[a]	V_{DS} = -5V, I_D = -4A	g_{fs}	--	6.5	--	S
Diode Forward Voltage	I_S = -0.75A, V_{GS} = 0V	V_{SD}	--	- 0.8	-1.2	V
Dynamic[b]						
Total Gate Charge	V_{DS} = -6V, I_D = -2.8A, V_{GS} = -4.5V	Q_g	--	5.4	10	nC
Gate-Source Charge		Q_{gs}	--	0.8	--	
Gate-Drain Charge		Q_{gd}	--	1.1	--	
Input Capacitance	V_{DS} = -6V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	447	--	pF
Output Capacitance		C_{oss}	--	127	--	
Reverse Transfer Capacitance		C_{rss}	--	80	--	
Switching[c]						
Turn-On Delay Time	V_{DD} = -6V, R_L = 6Ω, I_D = -1A, V_{GEN} = -4.5V, R_G = 6Ω	$t_{d(on)}$	--	5	25	nS
Turn-On Rise Time		t_r	--	19	60	
Turn-Off Delay Time		$t_{d(off)}$	--	95	110	
Turn-Off Fall Time		t_f	--	65	80	

Notes:
a. pulse test: PW =300μS, duty cycle =2%
b. For DESIGN AID ONLY, not subject to production testing.
b. Switching time is essentially independent of operating temperature.



Switching Test Circuit



Switchin Waveforms